Claims

1. Polyphase filter consisting of N branch allpass filters of order $x \cdot N$ to filter an input signal t(k), **characterized by**

- a structure of an allpass filter of order x comprising delay elements with a delay 1 and at least one multiplier, wherein all delay elements with a delay 1 are replaced by delay elements with a delay N, and

- a sampling rate $f_S' = f_S/N$, with f_S being the sampling rate of the input signal (t(k)).

2. Filter according to claim 1, **characterized in** that said at least one multiplier respectively comprises N time-multiplexed multiplication coefficients (α_0, ..., α_{N-1}; χ_0, ..., χ_{N-1}) that are used in a predetermined order ($\alpha(k)= \alpha_{(k \bmod N)}$; $\chi(k)= \chi_{(k \bmod N)}$).

3. Filter according to claim 1 or 2, **characterized by**:

- a first delay element (1) with a delay N that receives the input signal (t(k));

- a first adder (3) that receives the output signal of said first delay element (1) at a first input for the first summand;

- a second delay element (2) with a delay N that receives the sum produced by said first adder (3);

- a first subtracter (4) that receives the input signal (t(k)) at a first input for the minuend and the output signal of the second delay element (2) at a second input for the subtrahend; and

- a first multiplier (5) that receives the calculated difference of the first subtracter (4), multiplies it respectively with a predetermined multiplication coefficient ($\alpha(k)$) and outputs the calculated product to a second input of the first adder (3) that receives the second summand, wherein

- in case x equals to 1 the sum produced by said first adder (3) builds the output signal (u(k)) of the branch allpass filters.

4. Filter according to claim 3, **characterized by**:

- a second adder (6) that receives the output signal of the second delay element (2) at a first input for the first summand;

- a third delay element (7) with a delay N that receives the sum produced by said second adder (6);

- a second subtracter (8) that receives the sum produced by said first adder (3) at a first input for the minuend and the output signal of the third delay element (7) at a second input for the subtrahend; and

- a second multiplier (9) that receives the calculated difference of the second subtracter (8), multiplies it respectively with a predetermined multiplication coefficient ($\chi(k)$) and outputs the calculated product to a second input of the second adder (6) that receives the second summand, wherein

- in case x equals to 2 the sum produced by said second adder (6) builds the output signal (u(k)) of the branch allpass filters.

5. Filter according to anyone of claims 2 to 4, **characterized in** that every one of said at least one multipliers (5, 9) has quantised coefficients so that it can be realised by at least one shift register, at least one adder or at least one subtracter.

6. Filter according to claim 5, **characterized in** that one multiplier (5, 9) comprises:

- a first shift register (10) having a shift value of 2^{-2} that is receiving the multiplicand and,

- an input selector switch (S2) receiving the output value of said first shift register (10) at a first fixed input terminal and the multiplicand at a second fixed input terminal,

- a second shift register (11), a third shift register (12) and a fourth shift register (13) each having its input connected to the moveable output terminal of said input selector switch (S2),

- a third subtracter (14) receiving the output value of said second shift register (11) at a first input receiving the minuend,

- a first output selector switch (S3) having its moveable input terminal connected to the output of said third shift register (12), its first fixed output terminal runs free and its second fixed output terminal is connected to a second input of the third subtracter (14) receiving the subtrahend,

- a third adder (15) receiving the output value of said third subtracter (14) at a first input receiving the first summand and outputting the multiplied multiplicand,

- a second output selector switch (S4) having its moveable input terminal connected to the output of said fourth shift register (13), its first fixed output terminal runs free and its second fixed output terminal is connected to a second input of the third adder (15) receiving the second summand.

7. Filter according to anyone of the preceding claims, **characterized in that** a polyphase filter of order $x \cdot N$ with $x = a$ is realised in a time multiplex and works with a clock frequency $f_C = a \cdot f_S$.

8. IQ-generator, **characterized in that** an incoming sampled bandpass signal s(k) gets multiplied by a signal $A(k)=(-1)^{\text{floor }(k/N)}$ before being supplied as input signal t(k) to a polyphase filter consisting of N branch allpass filters (22) of order $x \cdot N$.

9. IQ-generator according to claim 8, **characterized in that** the output signal of the polyphase branch allpass filters (22) gets multiplied by a signal $B(k) \cdot \cos(2\pi f_0/f_S \cdot k)$ to calculate the I-component of the complex baseband signal and by a signal $B(k) \cdot \sin(2\pi f_0/f_S \cdot k)$ to calculate the Q-component of the complex baseband signal with $A(k)=B(k)=(-1)^{\text{floor}(k/n)}$.

10. IQ-generator according to claim 8 or 9, **characterized by** one polyphase filter according to anyone of claims 1 to 7 to filter the I-component and the Q-component of a complex baseband signal.